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10EC45

Fourth Semester B.E. Degree Examination, Dec.2014/Jan.2015
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the behavioral and dataflow style descriptions of VHDL, with the example of an half-adder. **(10 Marks)**

b. Compare VHDL and verilog. **(04 Marks)**

c. Explain structure of VHDL and verilog with an example. **(06 Marks)**

2 a. Write VHDL code for 2×2 bits combinational array multiplier (Dataflow style description). **(06 Marks)**

b. List the data types used in VHDL and verilog. **(04 Marks)**

c. Write a dataflow description in both VHDL and verilog, for a full adder with active high enable (en = 1). **(10 Marks)**

3 a. Distinguish between signal assignment and variable assignment statements in VHDL. Also, write VHDL program for behavioral description of D-latch using signal assignment and variable assignment statements, separately. **(10 Marks)**

b. Explain formats of for loop and while loop statements in both VHDL and verilog. **(06 Marks)**

c. Write VHDL code to calculate the factorial of positive integers. **(04 Marks)**

4 a. Write the structural description for full adder, using two half adders. **(06 Marks)**

b. Explain binding between two modules in verilog. **(04 Marks)**

c. Write VHDL structural description of 3-bits synchronous up counter using JK master slave flip-flops. **(10 Marks)**

PART – B

5 a. Give an example code for a procedure and a function. **(06 Marks)**

b. Write VHDL description of a full adder using procedure. **(08 Marks)**

c. Write a verilog code for converting a fraction binary to real using task. **(06 Marks)**

6 a. Why a mixed type description is needed? Write the VHDL code to find largest element in an array. **(10 Marks)**

b. Write a note on packages in VHDL. **(03 Marks)**

c. Write VHDL code for the addition of 5×5 matrices using a package. **(07 Marks)**

7 a. With a mixed language description of a full adder, explain the invoking of VHDL entity from a verilog module. **(10 Marks)**

b. Write the mixed language description of a JK master-slave flip-flop with clear input. **(10 Marks)**

8 a. What is meant by synthesis? List and explain steps involved in synthesis. **(07 Marks)**

b. Write VHDL or verilog code for the signal assignment statement y = 2 * a + 5 for an entity with one input a of 3-bits and one output y of 4-bits. Show the mapping of this signal assignment to gate level. **(10 Marks)**

c. Explain extraction of synthesis information from an entity. **(03 Marks)**

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